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09/750,476	12/28/2000	Victor Gutierrez de Dios	1961P	6589

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EXAMINER	
SHARON, AYAL I	

ART UNIT	PAPER NUMBER
2123	5

DATE MAILED: 08/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/750,476	DE DIOS ET AL.	
	Examiner	Art Unit	
	Ayal I Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,17-26,28,32-41 and 46-52* is/are rejected.

7)☒ Claim(s) *13-16,27,29-31 and 42-45* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. Claims 1-52 of U.S. Application 09/750,476 filed on 12/28/2000 are presented for examination.

Claim Objections

2. Claims 13-16, 27, 29-31, and 42-45 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and if the resulting claim were amended to overcome any 35 U.S.C. 112 issues.
3. Due to 35 U.S.C. 112 rejections, Claims 5-6, 21-22, 37-38, and 50-52 have not been rejected under the cited prior art. Claims 50-52 have also been rejected under 35 U.S.C. 101.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 46-52 rejected under 35 U.S.C. 101 because the disclosed invention is inoperative and therefore lacks utility. The preamble to Independent Claim 46 refers to "a computer readable medium with program instructions", however,

instructions need to be executed by a computer in order to be operative. This fact needs to be reflected in the claim.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 5-6, 21-22, 37-38, and 50-51 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The steps of "computing a construction for a multiple memory type module" and "computing an architecture for a multiple memory type module" in claims 5, 21, 37, and 50 are not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1-52 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter

which applicant regards as the invention. Independent claims 1, 17, 32, and 46 use the indefinite term "automatically". All dependent claims inherit this defect. In addition, dependent claims 4, 20-21, 37, and 49-50 also have the term "automatically" in the bodies of their claims.

10. The specification regarding the claimed invention is deficient in the areas cited above. Accordingly, the examiner has made prior art rejections based on the limited scope of information contained in the specification for supporting the claims. The rejections are complete and specifically applied against the claims based on this limited disclosure.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. The prior art used for these rejections is as follows:

13. Burrows et al., U.S. Patent 6,397,117. (Henceforth referred to as "**Burrows**").

14. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

15. Claims 1-2, 4, 7-12, 17-18, 20, 23-26, 28, 32-33, 35-36, 39-41, 46-47, 49, and 52 are rejected under 35 U.S.C. 102(e) as being anticipated by Burrows.

16. In regards to Claim 1, Burrows teaches the following limitations:

1. A method for providing a memory system design, comprising the steps of:
(a) receiving memory system criteria; and
(Burrows, especially: Fig.3, and col.4, lines 33-68; col.2, lines 57-65; col.3, lines 25-38; col.5, lines 11-18; col.6, line 65 – col.7, line 3; col.7, lines 39 – 41; col.8, lines 40-45;)

(b) automatically extracting at least one memory system design based upon the memory system criteria.
(Burrows, especially: Fig.3, and col.4, lines 33-68; col.2, lines 57-65; col.3, lines 25-38; col.5, lines 11-18; col.6, line 65 – col.7, line 3; col.7, lines 39 – 41; col.8, lines 40-45;)

17. In regards to Claim 2, Burrows teaches the following limitations:

2.The method of claim 1, wherein the receiving step (a) comprises:
(a1) providing a user interface; and
(Burrows, especially: Fig.3, and col.4, lines 33-68;col.2, lines 57-65; col.3, lines 25-38; col.5, lines 11-18; col.6, line 65 – col.7, line 3; col.7, lines 39 – 41; col.8, lines 40-45;)

(a2) receiving the memory system criteria via the user interface.
(Burrows, especially: Fig.3, and col.4, lines 33-68;col.2, lines 57-65; col.3, lines 25-38; col.5, lines 11-18; col.6, line 65 – col.7, line 3; col.7, lines 39 – 41; col.8, lines 40-45;)

18. In regards to Claim 4, Burrows teaches the following limitations:

4.The method of claim 1, wherein the automatically extracting step (b) comprises:
(b1) automatically processing the memory system criteria; and
(Burrows, especially: Fig.3, and col.4, lines 33-68;col.2, lines 57-65; col.3, lines 25-38; col.5, lines 11-18; col.6, line 65 – col.7, line 3; col.7, lines 39 – 41; col.8, lines 40-45;)

(b2) automatically extracting the at least one memory system design, wherein the at least one memory system design addresses the processed memory system criteria.
(Burrows, especially: Fig.3, and col.4, lines 33-68;col.2, lines 57-65; col.3, lines 25-38; col.5, lines 11-18; col.6, line 65 – col.7, line 3; col.7, lines 39 – 41; col.8, lines 40-45;)

19. In regards to Claim 7, Burrows teaches the following limitations:

7.The method of claim 1, further comprising:
(c) displaying the at least one memory system design.
(Burrows, especially: Fig.3, and col.4, lines 33-68;col.2, lines 57-65; col.3, lines 25-38; col.5, lines 11-18; col.6, line 65 – col.7, line 3; col.7, lines 39 – 41; col.8, lines 40-45;)

20. In regards to Claim 8, Burrows teaches the following limitations:

8.The method of claim 1, wherein the at least one memory system design comprises a multiple memory type module.
(Burrows, especially: col.5, lines 11-18;)

Examiner interprets Burrows's "memory cell" as corresponding to Applicants' "multiple memory type module".

21. In regards to Claim 9, Burrows teaches the following limitations:

9.The method of claim 8, wherein the multiple memory type module is comprised in at least one library, the at least one library comprising a plurality of multiple memory type modules.
(Burrows, especially: Fig.3, and col.4, lines 33-68;col.2, lines 57-65; col.3, lines 25-38; col.5, lines 11-18; col.6, line 65 – col.7, line 3; col.7, lines 39 – 41; col.8, lines 40-45;)

22. In regards to Claim 10, Burrows teaches the following limitations:

10.The method of claim 9, wherein the plurality of multiple memory type modules comprises different combinations of memory types, architectures, data bus widths, banking schemes, or performance and power characteristics.
(Burrows, especially: Fig.3, and col.4, lines 33-68;col.2, lines 57-65; col.3, lines 25-38; col.5, lines 11-18; col.6, line 65 – col.7, line 3; col.7, lines 39 – 41; col.8, lines 40-45;)

23. In regards to Claim 11, Burrows teaches the following limitations:

11. The method of claim 8, wherein the multiple memory type module comprises: a plurality of memory devices, comprising:
at least one of a first memory device of a first memory type,
(Burrows, especially: Fig.3, and col.4, lines 33-68;col.2, lines 57-65; col.3, lines 25-38; col.5, lines 11-18; col.6, line 65 – col.7, line 3; col.7, lines 39 – 41; col.8, lines 40-45;)

and at least one of a second memory device of a second memory type, wherein a minimum configuration of the plurality of memory devices consists of one memory device of the first memory type, and one or two memory devices of the second memory type;

(Burrows, especially: Fig.3, and col.4, lines 33-68;col.2, lines 57-65; col.3, lines 25-38; col.5, lines 11-18; col.6, line 65 – col.7, line 3; col.7, lines 39 – 41; col.8, lines 40-45;)

and a single memory bus coupled to the plurality of memory devices, wherein the single memory bus provides communication between a processor and the plurality of memory devices.

It is inherent that a memory device will be connected to a bus in order to communicate with other components.

24. In regards to Claim 12, Burrows teaches the following limitations:

12.The method of claim 11, wherein neither the first memory device nor the second memory device stores an identification data describing a device composition of the memory module.
(Burrows, especially: Fig.3, and col.4, lines 33-68;col.2, lines 57-65; col.3, lines 25-38; col.5, lines 11-18; col.6, line 65 – col.7, line 3; col.7, lines 39 – 41; col.8, lines 40-45;)

25. In regards to Claim 17, Burrows teaches the following limitations:

17.A system, comprising:

at least one library of multiple memory type modules, wherein the at least one library comprises:
(Burrows, especially: Fig.3, and col.4, lines 33-68;col.2, lines 57-65; col.3, lines 25-38; col.5, lines 11-18; col.6, line 65 – col.7, line 3; col.7, lines 39 – 41; col.8, lines 40-45;)

a single memory bus;

It is inherent that a memory device will be connected to a bus in order to communicate with other components.

a plurality of multiple memory type modules, wherein each of the plurality of multiple memory-type modules uses the single memory bus to communicate with a processor, wherein each of the plurality of multiple memory type modules comprises at least one of a first memory device of a first memory type and at least one of a second memory device of a second memory type; and
(Burrows, especially: Fig.3, and col.4, lines 33-68;col.2, lines 57-65; col.3, lines 25-38; col.5, lines 11-18; col.6, line 65 – col.7, line 3; col.7, lines 39 – 41; col.8, lines 40-45;)

a computer readable medium coupled to the at least one library, wherein the computer readable medium comprises program instructions for automatically providing a memory system design, the instructions for:
(Burrows, especially: Fig.3, and col.4, lines 33-68;col.2, lines 57-65; col.3, lines 25-38; col.5, lines 11-18; col.6, line 65 – col.7, line 3; col.7, lines 39 – 41; col.8, lines 40-45;)

(a)receiving memory system criteria, and
(Burrows, especially: Fig.3, and col.4, lines 33-68;col.2, lines 57-65; col.3, lines 25-38; col.5, lines 11-18; col.6, line 65 – col.7, line 3; col.7, lines 39 – 41; col.8, lines 40-45;)

(b)automatically extracting at least one memory system design from the at least one library based upon the memory system criteria.
(Burrows, especially: Fig.3, and col.4, lines 33-68;col.2, lines 57-65; col.3, lines 25-38; col.5, lines 11-18; col.6, line 65 – col.7, line 3; col.7, lines 39 – 41; col.8, lines 40-45;)

26. In regards to Claim 25, Burrows teaches the following limitations:

25.The system of claim 17, wherein a minimum configuration of each of the plurality of multiple memory type modules consists of

one memory device of the first memory type, and
(Burrows, especially: Fig.3, and col.4, lines 33-68;col.2, lines 57-65; col.3, lines 25-38; col.5, lines 11-18; col.6, line 65 – col.7, line 3; col.7, lines 39 – 41; col.8, lines 40-45;)

one or two memory devices of the second memory type.
(Burrows, especially: Fig.3, and col.4, lines 33-68;col.2, lines 57-65; col.3, lines 25-38; col.5, lines 11-18; col.6, line 65 – col.7, line 3; col.7, lines 39 – 41; col.8, lines 40-45;)

27. In regards to Claim 39, Burrows teaches the following limitations:

39. The method of claim 32, further comprising:

(d) displaying the at least one memory system design.
(Burrows, especially: col.5, lines 35-46)

28. In regards to Claim 40, Burrows teaches the following limitations:

40.The method of claim 32, wherein the multiple memory type module comprises:

a plurality of memory devices, comprising: at least one of a first memory device of a first memory type, and at least one of a second memory device of a second memory type, wherein a minimum configuration of the plurality of memory devices consists of: one memory device of the first memory type, and one or two memory devices of the second memory type; and
(Burrows, especially: Fig.3, and col.4, lines 33-68;col.2, lines 57-65; col.3, lines 25-38; col.5, lines 11-18; col.6, line 65 – col.7, line 3; col.7, lines 39 – 41; col.8, lines 40-45;)

a single memory bus coupled to the plurality of memory devices, wherein the single memory bus provides communication between a processor and the plurality of memory devices.

It is inherent that a memory device will be connected to a bus in order to communicate with other components.

29. **Claim 46 is rejected based on the same reasoning as claim 1, *supra*. Claim 46 is a medium claim that recites the equivalent limitations as are recited in method claim 1 and are taught throughout Burrows.**

30. **Claims 18, 20, 23-24, 32-33, 39, 47, 49, and 52 are rejected based on the same reasoning as claims 2, 4, and 7, *supra*. Claims 18 and 20-24 are systems claims, claims 32-33 and 37-39 are method claims, and claims 47, 49-52 are medium claims that recite the equivalent limitations as are recited in method claims 2, 4, and 7 and are taught throughout Burrows.**

31. **Claims 28 and 35-36 are rejected based on the same reasoning as claims 9-10, *supra*. Claim 28 is a systems claim and claims 35-36 are method claims that recite the equivalent limitations as are recited in method claims 9-10 and are taught throughout Burrows.**

Claim Rejections - 35 USC § 103

32. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

33. The prior art used for these rejections is as follows:

34. Burrows et al., U.S. Patent 6,397,117. (Henceforth referred to as "**Burrows**").

35. Crucial.com internet homepage, archived from Nov. 9, 1999. (Henceforth referred to as "**Crucial**").

36. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

37. Claims 3, 19, 34, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burrows in view of Crucial.

38. In regards to Claim 3, Burrows teaches the following limitations:

> 3.The method of claim 1, wherein the memory system criteria comprises: technical criteria; and
> (Burrows, especially: Fig.3, and col.4, lines 33-68;)

However, Burrows does not teach the following limitation:

> And market criteria.

Applicants define "Technical Criteria" and "Market Criteria" in the specification as follows (p.4, lines 11-17):

> Technical criteria includes, but is not limited to, the memory types needed, the minimum and maximum capacities of each memory type, the data bus width of each memory type, etc. They can also include a description of the processing units, performance specifications, environmental requirements, physical constraints, etc.
>
> Market criteria includes, but is not limited to, price, availability, and upgradability of various components. Based on these criteria, the automated memory design system 100 returns one or more solutions to the design engineer 104 from which the design engineer 104 may choose.

The archived copy of the Crucial.com internet homepage, on the other hand, enables the user to select the memory system in two different ways.

The first way is by "component type" (number of pins and type of memory, e.g. DIMM, SIMM, SODIMM). Examiner interprets this as corresponding to Applicants' "technical criteria", since the number of pins is a physical constraint.

The second way is by "manufacturer" (e.g. IBM, Intel, HP, Hitachi, Fujitsu). Examiner interprets this as corresponding to Applicants' "marketing criteria", since the differences between a similar component (e.g. 72-pin SIMM) made by two different manufacturers will not be technical in nature, but rather in terms of marketing (price, availability, etc.).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Burrows with those of Crucial, because doing so because Crucial's two ways to search for memory components are "easy" (see Crucial's slogan, "2 easy ways to buy memory!").

39. **Claims 19, 34, and 48 are rejected based on the same reasoning as claim 3, *supra*. Claims 19 is a systems claim, claim 34 is a method claim, and claim 48 is a medium claim that recite the equivalent limitations as are recited in method claim 3 and are taught throughout Burrows.**

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (703) 306-0297. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (703) 305-9704. Any response to this office action should be mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Hand-delivered responses should be brought to the following office:

4th floor receptionist's office
Crystal Park 2
2121 Crystal Drive
Arlington, VA 22202

Fax phone number is: (703) 872-9306

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is: (703) 305-3900.

Ayal I. Sharon

Art Unit 2123

August 20, 2004

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER